# CALLINAN 206-KFM 11122/U3625/CDM/td

### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

: RICHARD BISINELLA

Serial No. : TO BE ASSIGNED

Filed

HEREWITH

For

MICROPROCESSOR

February 2, 2001

Hon. Commissioner of Patents & Trademarks Washington, DC 20231

:

Sir:

#### PRELIMINARY AMENDMENT

Prior to examination, please amend the above-identified patent application as follows:

## IN THE CLAIMS:

On page 6, before line 1, delete "I CLAIM" and insert:

-- CLAIMS

What is claimed is: --

Please amend claims 1-5 as follows:

(Once Amended) [A] In a microprocessor having a program control and a plurality of circuit components [which are selected from] comprising registers, arithmetic logic units, memory[,] and input/output circuits [and other similar components commonly found in microprocessors, whereby] , the improvement wherein said plurality of components are

interconnected in a manner which allows connection between some of the components to be varied under <u>said</u> program control.

- 2. (Once Amended) The microprocessor as claimed in claim 1, wherein said plurality of components are interconnected on a grid [whereby] and wherein each of said plurality of components can be switched under said program control to be connected to a predetermined selection of one or more of said plurality of components.
- 3. (Once Amended) The microprocessor as claimed in claim 2, further including a grid connector which [provides] includes logic for interconnecting a predetermined one or more of said plurality of components with one or more other components of said plurality of components on said grid.
- 4. (Once Amended) The microprocessor as claimed in claim 1, wherein said plurality of components are interconnected on a grid [whereby] such that each of said plurality of components can be switched under said program control to be connected to a predetermined selection of one or more of said plurality of components, and further comprising an instruction set decoder for interpreting the instruction set of said microprocessor into timed signals to said components, a clock for timing operations of said

microprocessor and a grid connector which provides logic for interconnecting a predetermined one or more of said plurality of components with one or more other components of said plurality of components on said grid.

5. (Once Amended) The microprocessor as claimed in claim 2, further including at least one further grid of a plurality of interconnected further components [which are selected from] comprising registers, arithmetic logic units, memory, and input/output circuits [and other similar components commonly found in microprocessors, said at least one further grid of a plurality of further components whereby] wherein at least a part of said grid is coupled to at least a part of said at least one further grid.

## REMARKS

This Preliminary Amendment is being filed to place the claims in proper form under United States Patent Practice.

No new matter has been introduced.

Respectfully submitted,

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